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James R Foley, Reg No 39 979

WIRE DELAY DISTRIBUTED MODEL

Inventor

Alexander Tetelbaum
26867 New Dobbel Ave.
Hayward, CA 94542
Citizenship: Ukraine

Related Applications

This application claims the benefit of United States Provisional Application Serial No. 60/236,752, filed September 28, 2000, and United States Provisional Application Serial No. 60/236,902, filed September 28, 2000, and is a continuation in part of United States Patent Application Serial No. 09/771,272, filed January 26, 2001.

Background

This invention generally relates to the Elmore Model, and more specifically relates to enhancements to the Elmore Model so that wire delays can be more accurately estimated.

The Elmore Model is a mathematical model which is used to estimate the delays at tapping points along a RC line. In other words, it is a tool for estimating the delay associated with providing a signal over a wire to a capacitive load. The Elmore Model is widely used in circuit design. For example, the Elmore Model is widely used during construction of a balanced clock tree (BCT) at different levels of clock net partition. The Elmore Model is described in several publications. For example, see W.C. Elmore, "The transient response of damped linear networks with particular regard to wide-band amplifier", J Applied Physics, Vol. 19, no. 1, pp. 55-63, January 1948, and J. Vlach, "Numerical method for transient responses of linear networks with lumped, distributed or mixed parameters" Journal of the Franklin Institute, Vol. 288, No. 2, pp. 99-113, August 1969. Generally, one having ordinary skill the art is very familiar with the Elmore Model.

While the Elmore Model is a helpful model to use for wire delay estimations, the Elmore Model is not perfect, and very often introduces some error. In other words, the actual or real delay is often different than the delay as calculated using the Elmore Model. This error may be compounded when attempting to calculate skew using the Elmore Model, where one delay calculation is compared to another. Obviously, if the Elmore Model were to be improved or enhanced, estimations using the Elmore Model

would be more accurate. This would improve designs. For example, if the Elmore Model were to be improved or enhanced, clock skew can be minimized among partition groups in a balanced clock tree (BCT).

Additionally, in the prior art, when the Elmore Model is used to estimate the delay associated a clock buffer output, the output resistor of the clock buffer is not considered, and this impacts delay and clock skew estimations.

Objects and Summary

A general object of an embodiment of the present invention is to provide enhancements to the Elmore Model for more accurately estimating wire delays.

Another object of an embodiment of the present invention is to provide an improved method of using the Elmore Model to estimate the delay associated a clock buffer output, where the method includes taking into account the clock buffer output resistance.

Another object of an embodiment of the present invention is to provide a method of more accurately estimating delays using the Elmore Model, where the Elmore Model is based on a wire delay distributed model.

Briefly, and in accordance with at least one of the foregoing objects, an embodiment of the present invention provides an improved method of using the Elmore Model to estimate the delay which is associated with the a clock buffer output. The improved method provides that the clock buffer output resistor is taken into account when the Elmore Model is used to calculate the delay.

Preferably, the Elmore Model is used to estimate the delay associated with the clock buffer output without taking into account the clock buffer output resistance. Then, the Elmore Model is used to estimate the delay associated with the clock buffer output while taking into account the clock buffer output resistance. Then, the estimated delays are used to calculate the maximum skew error associated with the clock buffer output resistance. Estimated ramp values of the clock buffer input and output signals are used to calculate the value of the clock buffer output resistance.

Another embodiment of the present invention provides a method of using the Elmore Model to estimate wire delay, and the method includes the steps of formulating a distributed RC model, calculating an approximate delay based on the distributed RC model, calculating a capacitance value based on the approximate delay which has been calculated, and using the capacitance value in the Elmore Model to estimate the wire delay.

Brief Description of the Drawings

The organization and manner of the structure and operation of the invention, together with further objects and advantages thereof, may best be understood by reference to the following description, taken in connection with the accompanying drawings, wherein like reference numerals identify like elements in which:

FIGURE 1 is a schematic view of a representative arrangement where a length (l) of wire is used to supply a signal to a capacitive load (C_o);

FIGURE 2 is an RC model of that which is shown in FIGURE 1;

FIGURE 3 is an Elmore Model circuit based on that which is shown in FIGURES 1 and 2, wherein a clock buffer output resistor is not taken into account;

FIGURE 4 is an Elmore Model circuit which is in accordance with an embodiment of the present invention, wherein the clock buffer output resistor is taken into account;

FIGURE 5 shows the input and output leads of a clock buffer and signal parameters relating thereto;

FIGURE 6 is a schematic view relating to the estimation of skew error;

FIGURE 7 illustrates a distributed RC model;

FIGURE 8 illustrates a wire lumped model;

FIGURE 9 illustrates an RC circuit;

FIGURE 10 is an Elmore Model circuit which is in accordance with an embodiment of the present invention;

FIGURE 11 is a conventional or classical Elmore Model circuit; and

FIGURE 12 is a schematic view illustrating a balancing example.

Description

While the invention may be susceptible to embodiment in different forms, there are shown in the drawings, and herein will be described in detail, specific embodiments with the understanding that the present disclosure is to be considered an exemplification of the principles of the invention, and is not intended to limit the invention to that as illustrated and described herein.

A first embodiment of the present invention will now be described with reference to FIGURES 1-6. The embodiment provides that a clock buffer output resistor is calculated, and then the resistor is taken into account when using the Elmore Model to estimate delays and skew. This provides for more accurate estimations using the Elmore Model, as well as increases system performance and improves design quality.

FIGURE 1 depicts a representative arrangement 10 where a length (l) of wire is used to supply a signal to a capacitive load (C_o). An RC Model 20 of the arrangement is shown in FIGURE 2. The real theoretical delay for this RC circuit is:

(1) $D_{Real} = R\,C \ln 2 = 0.7\,R\,C$ or

(2) $D_{Real} = 0.7\,r\,l\,(c\,l + C_o)$ or

(3) $D_{Real} = 0.7\,r\,c\,l\,(1 + L_o)$

where r is the resistance and c is the capacitance of a unit length of wire, and $L_o = C_o / c$.

Illustrated in FIGURE 3 is the Elmore Model equivalent 30 of that which is shown in FIGURES 1 and 2, wherein the clock buffer output resistor is not taken into account. Mathematically applying the Elmore Model to that which is shown in FIGURE 3 provides:

(4) $D_{Without} = R\,(C/2 + C_o)$ or

(5) $D_{Without} = 0.5\, r\, c\, l\, (1 + L_o)$,

where r and c are unit length and capacitance, respectively, of the wire and is the resistance and c is the capacitance of a unit length of wire, and $L_o = C_o / c$.

FIGURE 4 shows an Elmore Model circuit 40 wherein the clock buffer output resistor (R_{out}) is taken into account. Mathematically applying the Elmore Model to that which is shown in FIGURE 4 provides:

(6) $D_{With} = R_{Out}\,(C + C_o) + D_{Without}$

The error in delay (Diff) as a result of not taking the clock buffer output resistor into account in the Elmore Model is effectively the difference between equations 4 and 6, or:

(7) $Diff = D_{With} - D_{Without} = R_{Out}\,(C + C_o)$.

FIGURE 5 shows the clock buffer input ("Input") and output ("Output") leads as well as illustrates the signal characteristics and parameters relating thereto (wherein "In" relates to the "Input" lead, and "Out" relates to the "Output" lead). With reference to FIGURE 5:

(8) $R_{Out} = 1000\ [t_{90}(C_{load}, t_{ramp}) - t_{50}(C_{load}, t_{ramp})] / C_{load} \ln 5$

(9) t_{ramp} ====> 0.3 → 0.5 (ramp time)

(10) $Diff = 621\ [t_{90}(C_{load}, t_{ramp}) - t_{50}(C_{load}, t_{ramp})]$.

For example, for clock buffer clkc16i, wherein:

$C_{load} = 5$ STDL

$t_{ramp} = 0.005$ ====>

$R_{out} = 404\ \Omega$

$Diff = 22.46 = const.$ (with 7.4 Ω error).

Then, the maximum skew error due to not accounting for the clock buffer output resistor can be estimated as follows, with reference to FIGURE 6:

(11) $E_s = 7.4\ |C1 - C2|$

(12) $E_s = 7.4\ c\ |l1 - l2|$

(13) $E_s = 0.0015\ |l1 - l2|$.

Thus, there is about 1.5 ps of skew error for each 1000μm of wire length. As a result of the significant error which results from not taking the clock buffer output resistor into account, it is important to, in accordance with the present invention, calculate the value of the clock output resistor, and to take the resistor into account when using the Elmore Model to estimate delay or skew. Additionally, it is apparent (from equations 12 and 13) that it would prove advantageous to use symmetrical routing (i.e., wherein l1 = l2).

Calculating the clock buffer output resistor and taking the resistor into account when using the Elmore Model to estimate delays and skew in accordance with the present invention provides for more accurate estimations using the Elmore Model. This increases system performance and improves design quality.

A second embodiment of the present invention will now be described with reference to FIGURE 1 and 7-12. The embodiment provides an improved method of using the Elmore Model to estimate wire delay, where the method includes steps of calculating an approximate delay based on a distributed RC model, and using a capacitance value corresponding to the approximate delay in the Elmore Model to estimate the wire delay. As a result, more accurate estimations can be made using the Elmore Model, and this increases system performance and improves design quality.

As discussed above, FIGURE 1 depicts a representative arrangement 10 where a length (l) of wire is used to supply a signal to a capacitive load (C_o). The present invention provides that a wire distributed model is used together with an Elmore Model. A distributed RC Model 50 is shown in FIGURE 7.

The step response of a uniform distributed RC wire is given in the Laplace domain by:

$$(14) \qquad V_{out} = \frac{V_{in}}{s\cosh(\sqrt{sRC})}$$

where C is the the total wire capacitance and R is the total wire resiatence.

The exact time domain response is given by the infinite series:

$$(15) \qquad V_{out}(t) = 1 - \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{(-1)^n}{2n+1}\exp\left[-\left(\frac{2n+1}{2}\pi\right)^2 \cdot \frac{t}{RC}\right]$$

which can be re-written as follows:

$$(16) \qquad V_{out}(t) = 1 - \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{(-1)^n}{2n+1}X^{-\left(\frac{2n+1}{2}\pi\right)^2}$$

where $X = e^{t/RC}$.

The delay $D_{distributed}$ of the RC distributed model can be found from the equation:

$$(17) \qquad V_{out}\,(D_{distributed}) = 0.5$$

A numerical solution is X = 1.460448 with 10^{-12} accuracy. Then

$$(18)\quad e^{D_{distributed}/RC} = X = 1.460448$$

and

$$(19)\quad D_{distributed} = RC \ln X = 0.3788243\ RC.$$

With 10^{-5} accuracy, only one member of the exact formula can be used as follows:

$$(20)\qquad V_{out}(t) = 1 - \frac{4}{\pi}\exp\left[-\left(\frac{\pi}{2}\right)^2 \cdot \frac{t}{RC}\right] = 0.5$$

Then, the approximate delay is:

$$(21)\qquad D'_{distributed} = RC\frac{\ln\left(\frac{\pi}{8}\right)}{-\left(\frac{\pi}{2}\right)^2} = 0.3788243RC$$

An improved Elmore Model for estimating the delay of a wire would preserve all Elmore delay properties and produce a more accurate estimation of eth delay according to the above-described theory. FIGURE 8 illustrates a Wire Lumped Model 60 wherein the exact value of the capacitors are C' = 0.3788243 C. Thus, instead of the total wire capacitance C (that is typically used in association with a conventional or classical Elmore Model), 2 * 0.3788243 C capaciatnce should be used to provide more accurate estimations.

The error associated with using a conventional or classical Elmore Model rather than an Elmore Model based on a distributed Rc model and modified capacitance values can be described as follows:

the delay along the wire is:

(22) $D_{distributed} = 0.3788243\ R\ C$, or

(23) $D_{distributed} = 0.3788243\ r\ c\ l^2$

where r is the unit length resistance of the wire and c is the unit capaciatnce of the wire and $L_o = C_o / c$.

The delay which is calculated using a conventional or classical Elmore Model is:

(24) $D_{Elmore} = RC/2$, or

(25) $D_{Elmore} = 0.5\ r\ c\ l^2$.

Hence, the error between the distributed delay and the Elmore delay is:

(26) $E(l) = D_{distributed} - D_{elmore}$

(27) $E(l) = -0.1211757\ r\ c\ l^2$

and the clock skew error is:

(28) $Es\ (l_1, l_2) = E(l_1) - E\ (l_2) = -0.1211757\ r\ c\ (l_1^2 - l_2^2)$.

With regard to a wire with a load, specifically an RC circuit 70 as shown in FIGURE 9, the theoretical 0.5 level delay is:

(29) $D_{Theory} = R\ C_o \ln 2 = 0.7\ R\ C_o$.

Hence, the load of the wire is introduced into an improved Elmore Model as:

$$(30)\quad C'_o = 0.7\, C_o.$$

Considering a wire with a nonzero load C_o, and substituting the wire with its improved Elmore Model value and the load with its improved value of 0.7 C_o, provides as shown in FIGURE 10. FIGURE 10 illustrates such an improved Elmore Model 80, wherein the Model is in accordance with the present invention.

The following illustrates how to find the difference between the new improved elay value (that is equal to the theoretical value) and delay associated with the conventional or classical Elmore Model:

$$(31)\quad D_{improved} = R\,(0.3788243C + 0.7\, C_o)$$

$$(32)\quad D_{improved} = r\, l\,(0.3788243\, c\, l + 0.7\, C_o)$$

$$(33)\quad D_{improved} = r\, c\, l\,(0.3788243l + 0.7\, L_o)$$

where r and c are unit length resistance and capacitance, respectively, of the wire and $L_o = C_o / c$. A conventional or classical Elmore Model 90 is shown in FIGURE 11, and the delay is:

$$(34)\quad D_{Elmore} = R\,(C/2 + C_o)$$

$$(35)\quad D_{Elmore} = r\, c\, l\,(0.5l + L_o).$$

The delay error is:

$$(36)\quad E(l) = D_{improved} - D_{elmore}$$

$$(37)\quad E(l) = -r\, c\, l\,(0.1211757\, l + 0.3\, L_o),$$

and the skew error is:

$$(38)\quad Es\,(l_1, l_2) = E(l_1) - E\,(l_2) = -r\, c\,[0.1211757\,(l_1^2 - l_2^2) + 0.3\, L_o\,(l_1 - l_2)].$$

Hence, it can be seen that for the classical Elmore Model a large $|l_1 - l_2|$ leads to big skew error and, therefore, a big skew. Minimization of $|l_1 - l_2|$ leads to skew minimization in all cases.

FIGURE 12 shows a balancing example 100 which approximates real designs. In FIGURE 12:

$r = 0.07$;

$c = 0.0002$;

$C_o = 4$ STDLs $= 0.0448$;

$Lo = 224$;

$l_1 = 7600$ and $l_2 = 1000$.

With reference to FIGURE 12,

(39) $D_{Elmore}(l_1) = r\, c\, l_1 (0.5\, l_1 + L_o) = 428ps$

(40) $D_{Elmore}(l_2) = r\, c\, l_2 (0.5\, l_2 + L_o) = 10ps$

(41) $D_{Elmore}(l_1) + D1 = D_{Elmore}(l_2) + D2 = 508ps$

(42) $D_{improved}(l_1) = r\, c\, l_1 (0.3788243\, l_1 + 0.7\, L_o) = 323ps$

(43) $D_{improved}(l_1) = r\, c\, l_2 (0.3788243\, l_2 + 0.7\, L_o) = 7.5ps$

(44) $D_{improved}(l_1) + D1 = 403ps$

(45) $D_{improved}(l_2) + D2 = 505.5ps$

(46) Skew Error = 505.5ps - 403ps =102.5ps

If two independent wires are considered, then:

$$(47) \qquad D_{improved} \approx \ln 2 \, D_{Elmore}$$

By using an improved Elmore Model in accordance with the present invention (i.e. by using a distributed model), more accurate delay and skew estimations can be made, and this increases system performance and improves design quality.

While embodiments of the present invention are shown and described, it is envisioned that those skilled in the art may devise various modifications of the present invention without departing from the spirit and scope of the appended claims.